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IMPROVING THE QUALITY OF THE 3-PHASE INVERTER USING A 5-LEVEL NEUTRAL POINT CLAMPED INVERTER TECHNIQUE COMBINED WITH THE SINUSOIDAL PULSE-WIDTH MODULATION

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Abstract – *The use of renewable energy sources is a global trend, aiming to limit the use of fossil energy sources that pollute the environment. Inverters are very important devices used in renewable energy conversion systems. Therefore, improving the quality of inverters is an issue that is receiving a lot of attention and research. This paper focuses on the solution to improve the quality of 3-phase inverters using the neutral point clamped (NPC)-5 level inverter technique combined with the sinusoidal pulse-width modulation (SinPWM) technique. One of the highlight points of this study is that it has successfully reduced the number of switching times and eliminated the common-mode voltage (CMV). The simulation results have shown that the proposed technique has achieved excellent and feasible results, thereby the inverter quality is significantly improved.*

Keywords: five-level inverter, multilevel inverter, NPC inverter, seven-level inverter, single-phase Inverter.

I. INTRODUCTION

In recent times, multi-level voltage source inverters have been increasingly applied in many industrial fields such as photovoltaic systems, fuel cell systems [1, 2], wind turbine systems, AC motor control [3–5], and power distribution systems [6]. These inverters are widely used because of their advantages such as high performance, low cost, and simple operation. Currently, inverter control methods have been increasingly implemented, specifically multi-level inverters, because they can create high-quality voltage waveforms with small total harmonic distortion (THD), low switching loss [7], and do not require a large output filter [8]. The main conditions for generating several different output voltage levels are to use multiple independent DC sources or to link virtual DC sources such as capacitors or transformers in combination with multiple switching devices [9].

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II. LITERATURE REVIEW

There are many techniques to create a multi-level inverter such as the neutral point clamped (NPC) [10], flying Capacitor [11], and cascade [12]. However, when using these inverters, there is also a disadvantage that comes with the generation of the common-mode voltage (CMV). This voltage negatively affects the performance of the inverter and reduces the life of the actuator. Therefore, there are many studies aimed at reducing CMV in inverters [13–18]. Specifically, Kim et al. [13] has shown that multi-level inverters with an odd number of levels have some switching vectors that do not generate or generate small CMVs, and performing the description of the desired voltage vector through this vector helps reduce or eliminate CMV. However, choosing vectors that do not generate CMV in some studies is still complicated. In addition, Tang et al. [14] have introduced a loss reduction method through phase-shifted carriers. Similarly, the problem of eliminating CMV on a 5-level cascade inverter based on the principle of using a key combination with a switching state that does not generate CMV has been demonstrated by Hai et al. [15].

Recently, Kim et al. [16] proposed a quite simple technique to suppress CMV is a switching sequence controlling the DC-DC converter to output CMV or using a simple dual-side zero-sequence voltage (ZSV) injection method based on carrier-based pulse-width modulation [17]. Besides, a way to reduce the CMV by using dual carriers was implemented by Guo et al. [18] and achieved encouraging results. However, most of these techniques have only been tested on 3-level inverters. Motivated by the above research works, this study focuses on research to improve the quality of 3-phase inverters with the novelties and main contributions of this study are as follows:

- The study proposed a three-phase 5-level NPC inverter combining pulse-width modulation technique - sinPWM.

- From the proposed model, a new modulation technique to reduce the number of switching times and suppress the CMV is introduced.

- Research results were verified through simulation with the support of PSIM software and it has shown that the system operates stably and that actual construction with digital signal processor (DSP) 28335 is feasible.

III. RESEARCH METHODS

The principle diagram of the 5-level NPC 3-phase inverter is shown in Figure 1, including eight insulated-gate bipolar transistors (IGBT) on each phase branch; four capacitors; and six clamped diodes on a phase.

Let u is the voltage on a capacitor, $T_{sx}, (x = a,b,c)$ is the state of the IGBTs of phase x, the switching diagram is presented in Table 1.

In which T_{sx} must satisfy the condition as in Expression (1).

$$T_{Sx} = \sum_{j=1}^{n-1} T_{Sxj}, \text{ and } T_{Sxj} + T'_{Sxj} = 1 \qquad (1)$$

Let $V_{xG}, (x = A,B,C)$ and V_{xN} are the DC source phase-center voltage and load center-phase voltage, respectively, they are determined by Expressions (2) and (3).

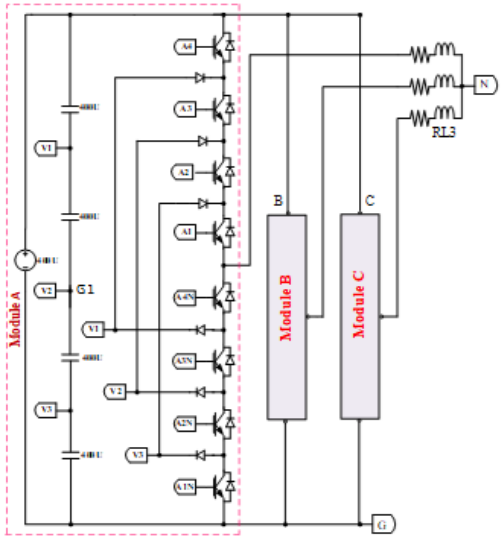

Fig. 1: The schematic of the 5-level NPC 3-phase inverter

Table 1: The switching sequence of IGBTs

No	U_{xG}	T_{Sx4}	T_{Sx3}	T_{Sx2}	T_{Sx1}	T'_{Sx4}	T'_{Sx3}	T'_{Sx2}	T'_{Sx1}
1	4u	1	1	1	1	0	0	0	0
2	3u	0	1	1	1	1	0	0	0
3	2u	0	0	1	1	1	1	0	0
4	u	0	0	0	1	1	1	1	0
5	0	0	0	0	0	1	1	1	1

$$\begin{bmatrix} V_{BG} \\ V_{AG} \\ V_{CG} \end{bmatrix} = \frac{u_{DC}}{n-1} \begin{bmatrix} T_{SA} \\ T_{SB} \\ T_{SC} \end{bmatrix} = u \begin{bmatrix} T_{SA} \\ T_{SB} \\ T_{SC} \end{bmatrix}, \qquad (2)$$

$$\begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} V_{AG} \\ V_{BG} \\ V_{CG} \end{bmatrix}, \qquad (3)$$

where u_{DC} is the DC source voltage supplied to the circuit, and n is the number of levels of the system.

Besides, the wire voltage is calculated as Expression (4).

$$\begin{bmatrix} V_{AB} \\ V_{BC} \\ V_{CA} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \end{bmatrix}. \qquad (4)$$

Let V_a, V_b, and V_c are the control voltages of phase A, phase B, and phase C, respectively.

These voltages have the same amplitude, frequency, and phase difference of 120^o, calculated by Expressions (5), (6), and (7).

$$V_a = A_m \sin(2\pi f_m t) + \frac{n-1}{2} A_c, \quad (5)$$

$$V_b = A_m \sin(2\pi f_m t - 120) + \frac{n-1}{2} A_c, \quad (6)$$

$$V_c = A_m \sin(2\pi f_m t - 240) + \frac{n-1}{2} A_c, \quad (7)$$

where A_m and f_m are the amplitude and frequency of the control voltage, respectively, and A_c is the carrier amplitude. The carrier waves are triangular waves and are represented by Expression (8).

$$cr_{i+1} = cr_i + 1, \ (i=1..4) \quad (8)$$

The cr_i carrier wave and control voltage will be fed into the comparator circuit. When the control voltage is greater than the carrier voltage, it will immediately turn on the IGBT. Conversely, if the control voltage is smaller than the carrier voltage, it will not turn on the IGBT. Figure 2 and Figure 3 respectively show the principle of on-off control of IGBTs according to control voltage and carrier wave.

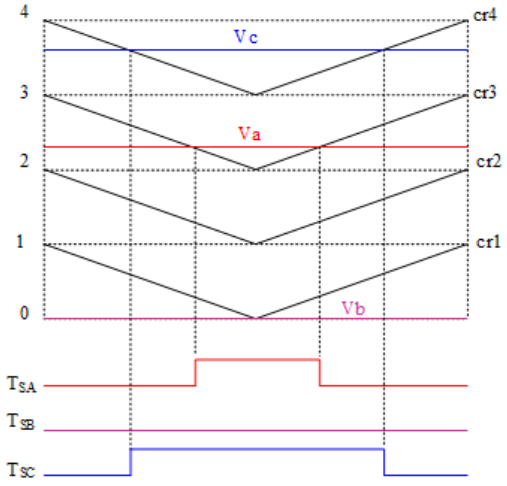

Fig. 2: Operating principle of IGBTs trigger circuit

In which T_{SA}, T_{SB}, and T_{SC} are the trigger pulses for the IGBTs of phase A, phase B, and phase C. According to Figure 2, there are four switching times.

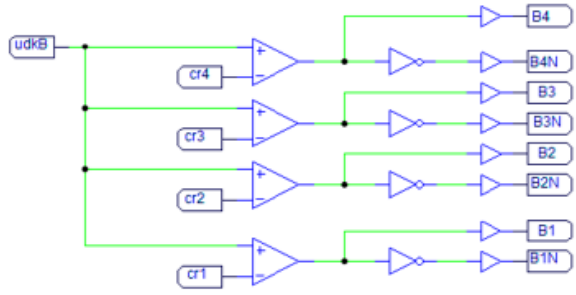

Fig. 3: The trigger pulse circuit for the IGBTs

A. Solution to reduce the number of switching times for the NPC 5-level inverter

Let $V_x, (x = a,b,c)$ is the initial $x-phase$ control voltage, and V_{xr} is the control voltage calculated from the algorithm to put into the modulation circuit. To reduce the number of switching times, that is, reduce switching losses, the main principle is to bring the control voltage V_x to the carrier thresholds throughout the cycle, so that the control voltage difference is minimal. It means that the control voltage value is always an integer multiple of the carrier amplitude $V_{rx} = kA_c, k \in N$ and $\overrightarrow{V_x} - \overrightarrow{V_{rx}} = min$.

Figure 4 describes the algorithm to reduce the number of switching times for the NPC 5-level inverter. The point '0' is chosen as the point corresponding to the bottom of the lowest carrier. The amplitudes of all triangular carriers are the same and equal to 1. At this time, the switching comparison thresholds will be 0, 1, 2, 3, and 4 because it is using a 5-level inverter.

Let m be the modulation index, and the value of m is defined as Expression (9).

$$m = \frac{V_{rx}}{\frac{(n-1)A_c}{2}} \frac{\sqrt{3}}{2} = \frac{V_{rx}\sqrt{3}}{n-1} = \frac{V_{rx}\sqrt{3}}{4}. \quad (9)$$

At this time, voltage is rewritten as Expression (10).

$$V_x = V_{rx}\sin(\omega t + j_x) + V_{offset}, \quad (10)$$

where the V_{offset} voltage is determined according to the goal of reducing CMV. Therefore, the control voltages for phases A, B, and C are calculated as Expression (11).

$$\begin{aligned} V_a &= m\frac{n-1}{\sqrt{3}}\sin(\omega t) + V_{offset} \\ V_b &= m\frac{n-1}{\sqrt{3}}\sin(\omega t - 120^\circ) + V_{offset} \\ V_c &= m\frac{n-1}{\sqrt{3}}\sin(\omega t - 240^\circ) + V_{offset} \quad (11) \\ V_{offset} &= \frac{n-1}{2} = 2 \text{ is chosen.} \end{aligned}$$

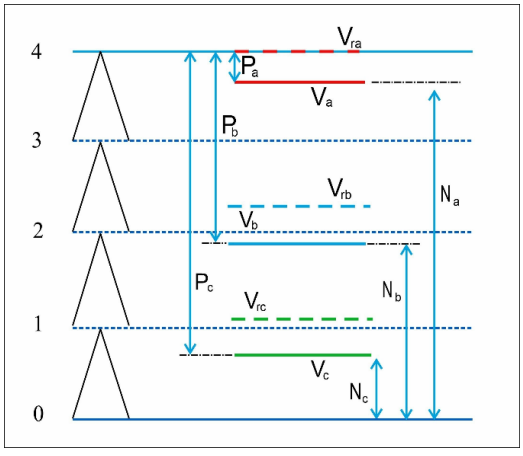

Fig. 4: Description of the algorithm

Let P_x and $N_x, (x = a,b,c)$ are the voltage difference between phase x compared to the top and bottom voltage thresholds of the carrier, respectively. Similarly, let H_x and L_x be the upper and lower threshold voltages closest to V_x for comparison of phase x, respectively, and they are defined as Expressions (12) and (13).

$$\begin{aligned} L_x &= \begin{cases} \text{int}(V_x) & \text{if } V_x \le n-1 \\ \text{int}(V_x) - 1 & \text{else} \end{cases} \\ H_x &= L_x + 1, \quad (12) \\ N_x &= V_x - L_x, \\ P_x &= L_x + 1 - V_x, \\ MinN &= Min(N_a, N_b, N_c), \\ MinP &= Min(P_a, P_b, P_c), \quad (13) \end{aligned}$$

in which, int(V_x) is the integer part of V_x.

Therefore, the V_{offset} voltage is determined as Formula (14).

$$V_{offset} = \begin{cases} MinP \text{ if } MinP < MinN, \\ -MinN \text{ if } MinP \ge MinN. \end{cases} \quad (14)$$

From the above analysis, an algorithm is obtained to reduce the number of switching times as shown in Table 2.

Table 2: The algorithm to reduce switching times

	Reduce switching times algorithm
1:	**Begin**
2:	*Enter the control voltage value Va, Vb, Vc, m;*
3:	*Calculate the values of Lx:*
4:	***if*** $(V_x \le 4)$ ***then***
5:	$L_x = \text{int}(V_x)$
6:	***else***: $L_x = \text{int}(V_x) - 1$
7:	*Calculate the values of* N_x, P_x *:*
8:	$N_x = V_x - L_x$ $P_x = L_x + 1 - V_x$
9:	$MinN = Min(N_a, N_b, N_c)$ $MinP = Min(P_a, P_b, P_c)$
10:	***if*** $(MinP < MinN)$ ***then***:
11:	$V_{offset} = MinP$
12:	***else:*** $V_{offset} = -MinN$
13:	$V_{rx} = V_x + V_{offset}$
14:	**end**

B. 5-level NPC inverter using IC F28335 – CMV suppression

The CMV of the inverter circuit is the voltage between the load center and the DC source supplying the system. The CMV affects the current of the AC motor and reduces the life of the motor. Although the goal of reducing the number of switching times has been achieved successfully, it still exists CMV. Therefore, in this subsection, we study the solution to suppress CMV, with a pulse generation circuit for IGBT using DSP F28335 as shown in Figure 5.

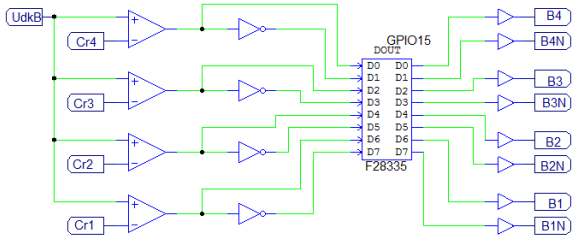

Fig. 5: The trigger pulse circuit for the IGBTs using F28335

Let V_{NG1} is the CMV, also known as the load center-source voltage, it is determined by Expression (15).

$$V_{NG1} = V_{NG} - \frac{u_{DC}}{2} = \frac{V_{AG} + V_{BG} + V_{CG}}{3} - \frac{u_{DC}}{2}. \quad (15)$$

The CMV has a value of 0 when it satisfies the condition shown in Expression (16).

$$T_{SA} + T_{SB} + T_{SC} = \frac{3(n-1)}{2}. \quad (16)$$

Therefore, for a 5-level inverter, to eliminate the CMV, the following condition in Expression (17) must be satisfied.

$$T_{SA} + T_{SB} + T_{SC} = 6. \quad (17)$$

Thus, the CMV is the result of the switching process when performing PWM. With a 2-level inverter, there are no CMV suppression states. However, with multi-level inverters, there will be states where CMV does not arise, which allows for eliminating CMV in the inverter circuit. To eliminate CMV several hardware designs have been proposed with the use of passive or active devices. Compared to applying hardware, applying the PWM algorithm to eliminate CMV will be more economical.

The principle of the algorithm is to bring the control voltage Vx to the carrier thresholds throughout the cycle to reduce losses, and the control voltage vector is the vector that does not generate CMV when performing switching. That is, the control voltage value is always an integer multiple of the carrier amplitude $v_{rx} = KA_c, K \in N$ and $v_{ra} + v_{rb} + v_{rc} = 6$.

With the above analysis, the control voltage V_x is now separated into two components, the integer part is L_x and the residual part is ε_x, calculated by Expressions (18), (19) and (20), respectively.

$$V_x = L_x + \varepsilon_x, 0 \le \varepsilon_x < 1. \quad (18)$$

Let:

$$\begin{aligned} \varepsilon_{\max} &= \max(\varepsilon_a, \varepsilon_b, \varepsilon_c), \\ \varepsilon_{\min} &= \min(\varepsilon_a, \varepsilon_b, \varepsilon_c), \end{aligned} \quad (19)$$

$$\begin{aligned} F_x &= \varepsilon_a + \varepsilon_b + \varepsilon_c \\ &= 6 - (L_a + L_b + L_c), \end{aligned} \quad (20)$$

where F_x is the total residual of the V_x.

At this time, three cases can happen as described in Expressions (21), (22) and (23) as follows:

Case 1: ε_x can be derived as:

$$\Rightarrow V_x = L_x \quad (21)$$

Case 2: When two of the three values ε_a, ε_b, ε_c are smaller than 0.5, it can be obtained as $\varepsilon_a + \varepsilon_b + \varepsilon_c = 1$ and $L_a + L_b + L_c = 5$.

$$\Rightarrow V_x = \begin{cases} L_x \text{ if } \varepsilon_{\max} > \varepsilon_x, \\ H_x \text{ if } \varepsilon_{\max} = \varepsilon_x. \end{cases} \quad (22)$$

Case 3: When two of the three values ε_a, ε_b, ε_c are larger than 0.5, they can be obtained as $\varepsilon_a + \varepsilon_b + \varepsilon_c = 2$ and $L_a + L_b + L_c = 4$.

With the above analysis, the CMV suppression algorithm was obtained as shown in Table 3.

Table 3: The VCM suppression algorithm

	CMV suppression algorithm
1:	**Begin**
2:	*Enter the control voltage value Va, Vb, Vc, m;*
3:	*Calculate the values of Lx and Hx:*
4:	***if*** $(V_x \le 4)$ ***then***
5:	$L_x = \text{int}(V_x)$
6:	***else***: $L_x = \text{int}(V_x) - 1$
7:	***end if***
8:	$H_x = L_x + 1$
9:	*Calculate the values of* ε_x *:*
10:	$\varepsilon_x = V_x - L_x$
11:	*find the* $\varepsilon_{\max}$ *and* $\varepsilon_{\min}$ *:*
12:	$\varepsilon_{\max} = \max(\varepsilon_a, \varepsilon_b, \varepsilon_c)$ $\varepsilon_{\min} = \min(\varepsilon_a, \varepsilon_b, \varepsilon_c)$
13:	Let: $Sum1 = L_a + L_b + L_c$ $Sum2 = Sum1 + 1$ $Sum3 = Sum1 + 2$ $Sum4 = H_a + H_b + H_c$
14:	***if*** $(Sum1 == 6)$ ***then***:
15:	$V_x = L_x$
16:	***elseif*** $(Sum2 == 6)$ ***then***:
17:	*if* $(\varepsilon_{\max} > \varepsilon_x)$ then $V_x = L_x a$
18:	*if* $(\varepsilon_{\max} == \varepsilon_x)$ then $V_x = H_x$
19:	***elseif*** $(Sum3 == 6)$ ***then***:
20:	*if* $(\varepsilon_{\min} = \varepsilon_x)$ then $V_x = L_x$
21:	*if* $(\varepsilon_{\min} < \varepsilon_x)$ then $V_x = H_x$
20:	***elseif*** $(Sum4 == 6)$ ***then***:
22:	$V_x = H_x$
23:	***else*** *break;*
24:	***end if***
25:	**End**

IV. RESULTS AND DISCUSSION

In this section, the research results will be verified through simulation with the support of psim software. The simulation parameters are presented in Table 4.

Figure 6 and Figure 7 show the output voltage and current of the NPC inverter at $m = 0.866$, respectively. The output signal has a sinusoidal shape with five levels. The THD measured in this

Table 4: The simulation parameters

Parameters	Value
DC voltage	400 V
Carrier frequency	5 KHz
Output voltage frequency	50 Hz
Load R/L	$200\Omega / 20mH$

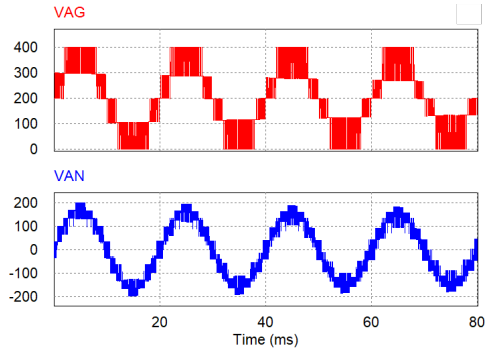

Fig. 6: Voltage output of 5-level NPC inverter

case is 1.6%. However, the number of switching times is still quite high, causing large losses and reducing the life of the components. To solve this problem, a solution to reduce the number of switching times has been proposed, with the results shown in Figure 8.

Although the number of switching times has been significantly reduced, the CMV still exists as shown in Figure 9. Therefore, research on eliminating CMV is carried out and results are shown in Figure 10 and 11, with the modulation indices $m = 0.866$ and $m = 1$, respectively.

The simulation results before and after applying the algorithm suppress the CMV at the presented m values presented in Table 5.

Table 5 shows that the voltage values will increase as m increases and vice versa for THD. Although the proposed algorithm eliminates the CMV, the THD is higher than a conventional inverter, which reduces the energy conversion efficiency.

The previous research results have demonstrated that the proposed model achieves superior energy conversion efficiency. Since IGBTs only get half of the DC bus voltage, NPC 5-level inverters are better suited for greater-power un-

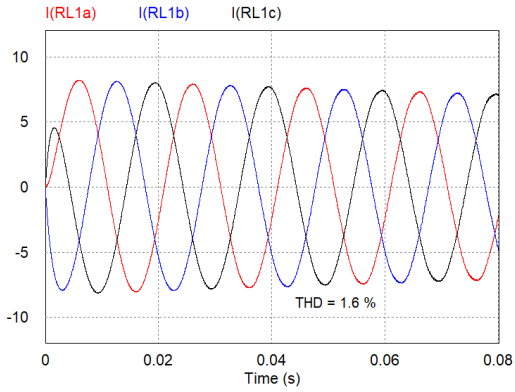

Fig. 7: Currents output of 5- level NPC inverter

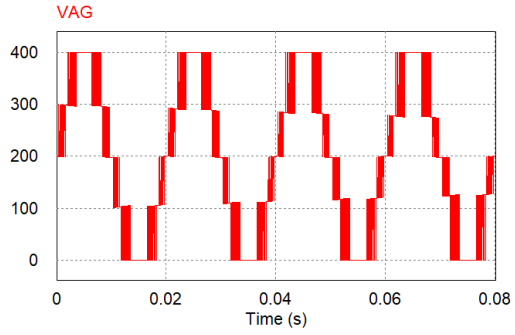

Fig. 8: The output voltage has reduced the number of switching times

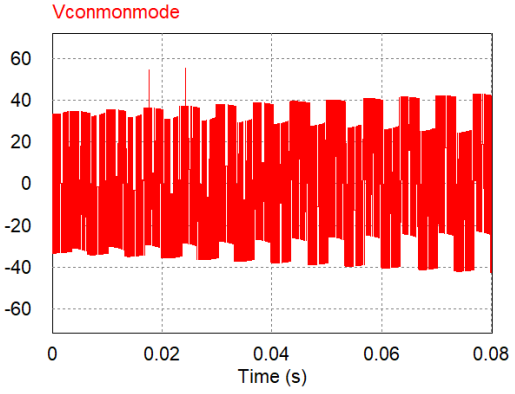

Fig. 9: The common mode voltage when the number of switching times has been reduced

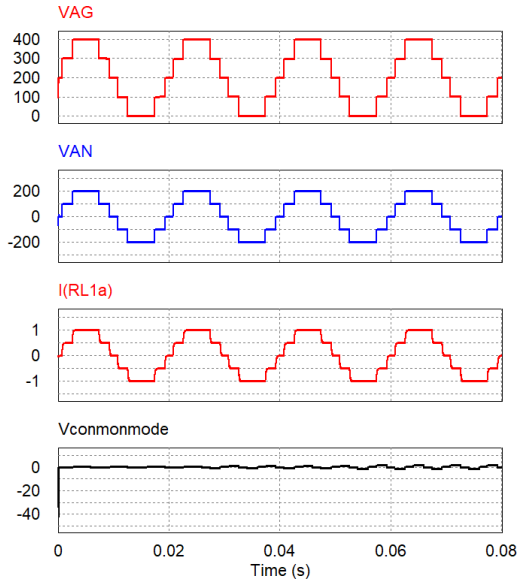

Fig. 10: The output signal suppresses the CMV when $m = 0.866$

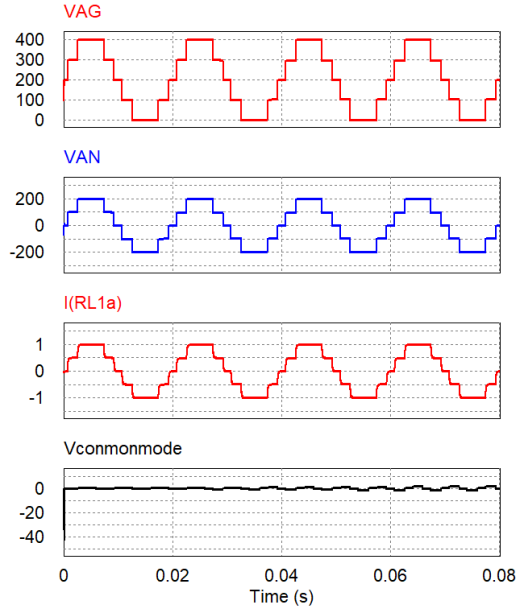

Fig. 11: The output signal suppresses the CMV when $m = 1$

Table 5: Comparison of conventional inverter and proposed method

m	0.866	1.0	Method
V_{AN}	116.85	139.2	Conventional
V_{AG}	235.7	245.2	
V_{NG1}	40.1	31.6	
THD %	1.6	1.16	
V_{AN}	117.8	140.3	Reduce switching
V_{AG}	234.4	245.1	
V_{NG1}	33.9	27.2	
THD %	2.7	1.2	
V_{AN}	120.2	151.1	Suppress CMV
V_{AG}	233.4	250.7	
V_{NG1}	0	0	
THD %	28.9	14.6	

interruptible power supply. Saving voltage-rated IGBT modules can save costs while reducing the system's power losses. Furthermore, it is easy to see that the proposed 5-level NPC inverter model provides better AC voltage conversion quality than the 2-level inverter [6] and 3-level inverter [11, 14].

V. CONCLUSION

The paper has successfully researched and simulated the NPC 5-level inverter using the SinPWM modulation technique. The novel of this research is the proposed technique to reduce the number of switching times and successfully eliminate CMV. Therefore, the quality of the NPC inverter has been significantly improved. Simulation results have shown that the system operates well, stably, and meets the requirements for a basic inverter. For further works and related research topics in the future, the proposed technique will be applied to implement a practical inverter, as well as further increase level of the inverter.

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